

POSZ LAW GROUP, PLC

ATTORNEYS AT LAW

12040 SOUTH LAKES DRIVE, SUITE 101
RESTON, VA 20191TEL: (703) 707-9110
FAX: (703) 707-9112

WWW.POSZLAW.COM

DEBRA G. SHOEMAKER, PH.D.^{**}
TERESI YOSHIDA +** PATENT AGENT
+ JAPANESE PATENT ATTORNEY
ADMITTED ONLY IN JAPANDAVID G. POSZ
JAMES M. ALPERT^{*}
BRIAN C. ALTMILLER
CYNTHIA K. NICHOLSON
THERESA B. VARNDELL^{*}
JAMES M. ALPERT^{*}^{*} NOT ADMITTED IN VIRGINIA
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To: Examiner Jean B. Corrielus

From: Brian C. Altmiller

RE: Proposed Claim Amendments for 10/538,174

Comments:

Examiner Corrielus,

Please see the attached proposed claim amendments for application serial no. 10/538,174, which we discussed earlier today. If you believe that after entering these claim amendments the application will be in condition for allowance, please enter them by Examiner's Amendment.

If you have any questions, or wish to discuss the matter any further, please give me a call at (703) 707-9110.



Brian C. Altmiller

Appl. No.: 10/538,174

Confirmation No.: 1753

Applicant: MILLER et al.

Filed: 9 June 2005

TC/A.C.: 2611

Examiner: CORRIELUS, JEAN B.

Docket No.: 10X-196/XSI.076

Customer No.: 51204

ENTITLED: DECISION FEED FORWARD EQUALIZER SYSTEM AND METHOD

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Proposed Claim Amendments for 10/538,174

6. (Currently Amended) The equalizer of claim 5 wherein each of the N_f feed forward circuits further comprises a corresponding circuit coupled to the delay line and operable to provide a corresponding hard decision according to a polarity of a signal at the input of a corresponding one of the any one of the series coupled delay circuits, and a corresponding scaling circuit operable to associate the polarity with the scaling factor to provide a corresponding one of the N_f feed forward signals and the output combiner is a summer that provides a linear combination of the N_f feed forward signals and the interim signal as the output signal.

7. (Currently Amended) The equalizer of claim 5 wherein each of the N_b feedback circuits further comprises a circuit coupled to the delay line and operable to provide an other hard decision corresponding to a polarity of a signal at the output of a corresponding one of the any one of the series coupled delay circuits, and a scaling circuit operable to associate the polarity with the other scaling factor to provide a corresponding one of the N_b feedback signals and the input combiner is a summer that provides a linear combination of the N_b feedback signals and the input signal to provide the signal at the first input of the series coupled delay circuits.